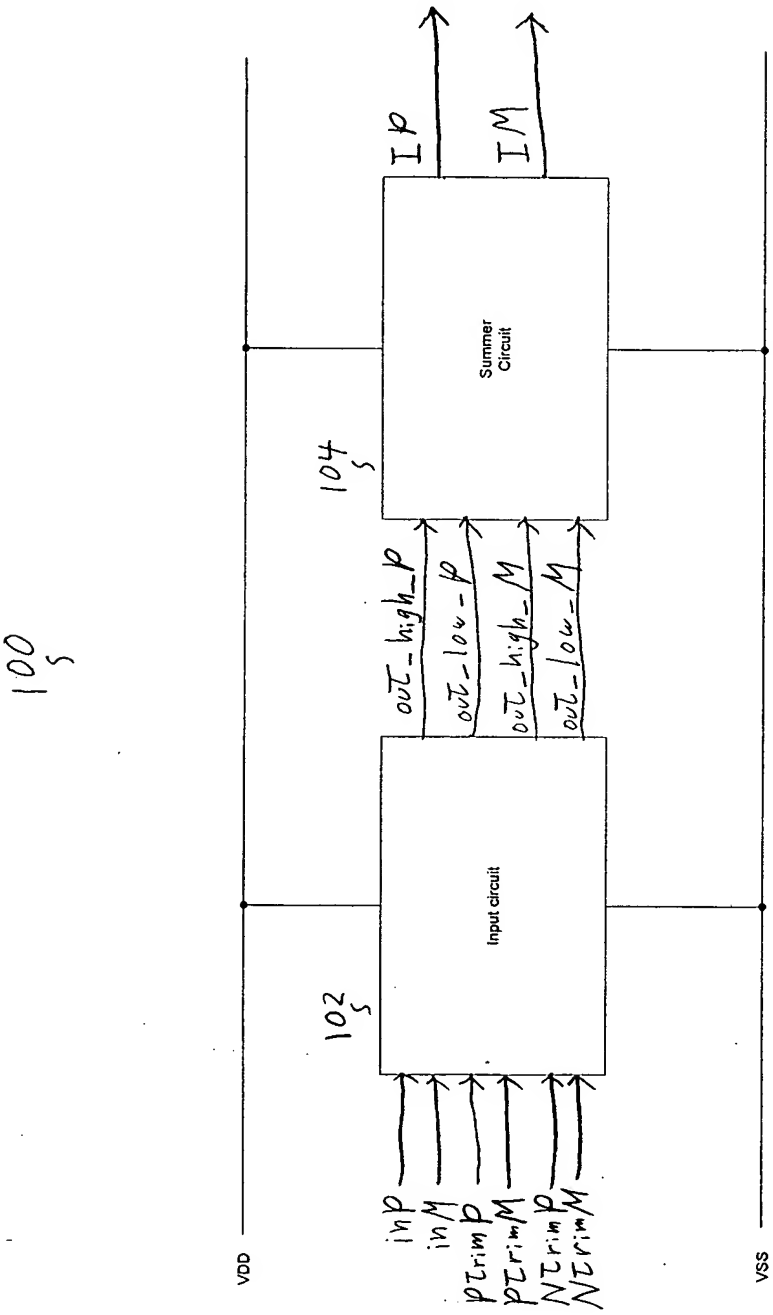
100
Summer Circuit
104
Input circuit
102
IP
IM
out_high_P
out_low_P
out_high_M
out_low_M
inP
inM
pTrimP
pTrimM
NTrimP
NTrimM
VDD
VSS

FIG. 1

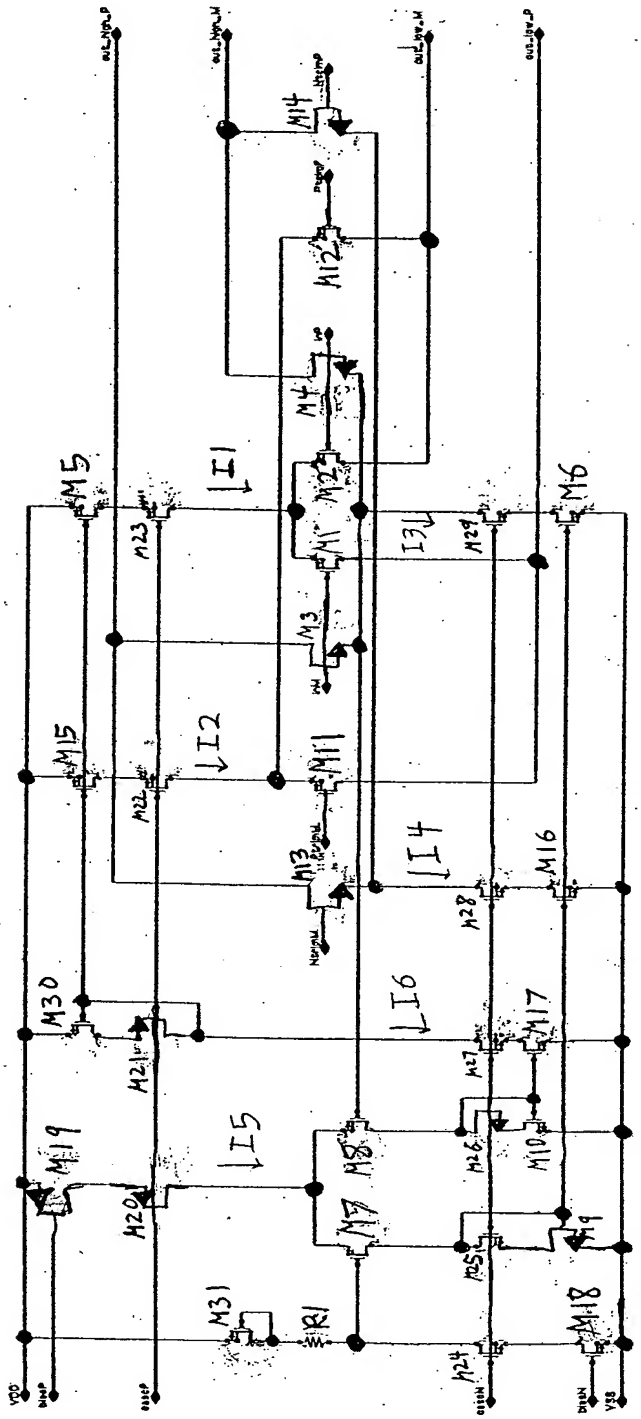
102
S
M14
M12
M4
M2
M5
I1
M23
M1
I3
M29
M6
M3
M15
I2
M22
M11
M13
I4
M28
M16
M30
I6
M17
M21
M27
M19
I5
M8
M26
M10
M20
M7
M9
M25
M31
R1
M24
M18
VDD
VSS

FIG. 2